Notice of Allowability	Application No.	Applicant(s)	
	10/532,367	OSHIMA, HIDEYUKI	
	Examiner	Art Unit	
	STEVEN D. RADOSEVICH	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/20/05*.

2. ☒ The allowed claim(s) is/are *1-4*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4/20/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *2/29/08* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

DETAILED ACTION

Claims 1-4 are present within this initial examination.

Priority

Acknowledgment is made that foreign priority is claimed to Japan document 2002-310146 with a date of 10/24/2002. Therefore the date used within this examination is reflective of this priority and the date 10/24/2002 is being used within this examination.

Information Disclosure Statement

Acknowledgment is made that an Information Disclosure Statement (IDS) was filed prior to this examination and as such the contents of the IDS has been reviewed at this time. Examiner notes that three foreign Japanese patent documents comprise the IDS.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Yasuo Muramatsu on 2/29/2008.

The application has been amended as follows:

With respect to the claims, claim 3 has been amended to appropriately identify the limitations included within the limitation of the search circuit to read as follows:

3 A semiconductor test apparatus comprising:

a reference clock generation unit which generates a reference clock signal;

a test pattern generation unit which outputs a test pattern signal applied to a semiconductor device in synchronization with the reference clock signal;

a timing generation unit comprising a variable delay circuit which delays the test pattern signal by a predetermined time;

a comparison unit which compares a response output signal output from the semiconductor device with an expected value pattern; and

a search circuit comprising:

a storage section which stores a target value;

a delay amount measurement section which obtains a delay amount measured value of the test pattern signal;

a tentative target value calculation section which extracts the target value from the storage section and which calculates, as a tentative target value, a value obtained by subtracting a predetermined value from the extracted target value or adding the predetermined value thereto;

a binary search executing section which applies a delay amount set value of the variable delay circuit in such a manner as to limit a searching range to a certain region including the tentative target value by binary search;

a sequential search executing section which applies the delay amount set value of the variable delay circuit in such a manner as to search for the target value in an increasing or decreasing direction from the tentative target value which is a start point in the limited searching range by sequential search;

a VD setting section which sets a delay amount of the variable delay circuit; and

a search control section which sends the tentative target value and the delay amount measured value to the binary search executing section and which sends the delay amount set value from the binary search executing section to the VD setting section to set the delay amount of the variable delay circuit and which sends the delay amount set value, the target value, and the delay amount measured value, obtained by limiting, to the sequential search executing section, when the searching range is limited to the certain region including the tentative target value and which sends the delay amount set value from the sequential search executing section to the VD setting section to set the delay amount of the variable delay circuit.

With respect to the Drawings, the following changes to the drawings have been approved by the examiner and agreed upon by applicant: Figures 5-10 are to be labeled or have the legend of --Prior Art-- since that which is illustrated within these figures is

old. In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

Claims 1-4 are allowable.

The present invention pertains to searching for a target value through the combination of a binary search and sequential search (linear search). The claimed invention recites features such as: "a target value storage section which stores a target value; a search control section which extracts the target value from the target value storage section and which sets, as a tentative target value, a value obtained by subtracting a predetermined value from the extracted target value or adding the predetermined value thereto; a binary search executing section which limits a searching range to a certain region including the tentative target value by binary search; and a sequential search executing section which searches for the target value in an increasing or decreasing direction from the tentative target value which is a start point in the limited searching range by sequential search."

The closest prior arts, Wang et al (U.S. Publication 20020138801 A1) and Kizer et al (U.S. Patent 6911853), both teaches the combination of a linear search (a.k.a. sequential search) with a binary search for reducing the diagnosis time or locating of the target value; wherein the binary search is used to reduce the search range for a linear search to locate the target value. None of the closest prior arts, either taken by itself or in any combination, would have anticipated or made obvious the following limitations

within the above limitations at or before the time the invention as filed: “a search control section which extracts the target value from the target value storage section and which sets, as a tentative target value, a value obtained by subtracting a predetermined value from the extracted target value or adding the predetermined value thereto; a binary search executing section which limits a searching range to a certain region including the tentative target value by binary search; and a sequential search executing section which searches for the target value in an increasing or decreasing direction from the tentative target value which is a start point in the limited searching range by sequential search."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN D. RADOSEVICH whose telephone number is (571)272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACQUES H LOUIS-JACQUES/
Supervisory Patent Examiner, Art Unit 2117

Steven D. Radosevich
Examiner
Art Unit 2117